	TET ESTEL AS ESTONIA	**June 2013**

Series
T151-100

Phase Control Stud Mounted Thyristor
Type T151-100

Center amplifying gate
Low on-state and switching losses
Designed for traction and industrial applications

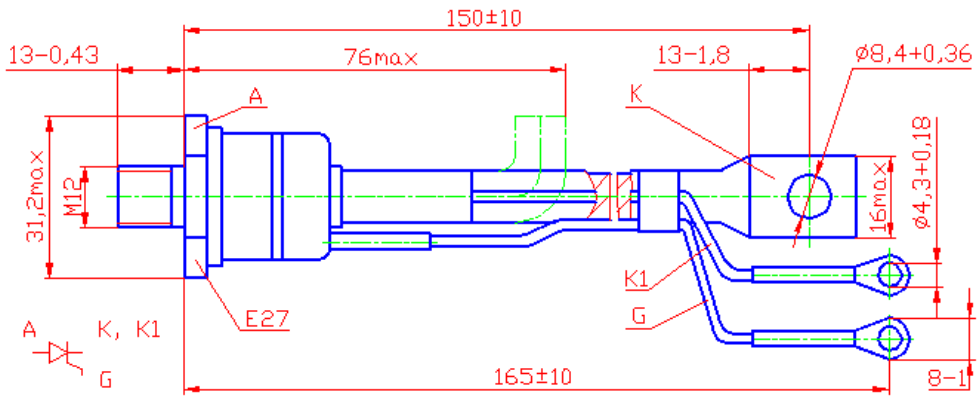
Maximum mean on-state current					I_{TAV}	**100 A**			
Maximum repetitive peak off-state and reverse voltage					U_{DRM} U_{RRM}	**800 ÷1600 V**			
Turn-off time					**tq**	**100; 160; 250 µs**			
U_{DRM}, U_{RRM}, V	800	900	1000	1100	1200	1300	1400	1500	1600
Voltage code	8	9	10	11	12	13	14	15	16
Tvj, °C	- 60 ÷ 125								

MAXIMUM ALLOWABLE RATINGS					
Symbols and parameters		Units	T151-100	Conditions	
I_{TAV}	Mean on-state current	A	100	Tc=90 °C, 180° half-sine wave, 50 Hz	
I_{TRMS}	RMS on-state current	A	157	Tc=90 °C	
I_{TSM}	Surge on-state current	kA	2,0 2,2	Tvj=125°C Tvj=25°C	tp=10 ms U_R=0
I^2t	Limiting load integral	kA^2s	20 24,2	Tvj=125°C Tvj=25°C	
U_{DRM},U_{RRM}	Repetitive peak off-state and reverse voltage	V	800÷1600	Tj min≤Tvj≤Tjm 180° half-sine wave, 50 Hz Gate open	
U_{DSM},U_{RSM}	Non-repetitive peak off-state and reverse voltage	V	900÷1700	Tj min≤Tvj≤Tjm 180° half-sine wave tp=10 ms, Single pulse Gate open	
(di$_T$/dt) crit	Critical rate of rise of on-state current : non - repetitive repetitive	A/µs	 250 125	Tvj=125°C ; U_D=0,67 U_{DRM}, Gate pulse : 10V,5 Ω, 1µs rise time, 10 µs	
U_{RGM}	Peak reverse gate voltage	V	5	Tj min≤Tvj≤Tjm	
Tstg	Storage temperature	°C	-60÷80		
Tvj	Junction temperature	°C	-60÷125		
CHARACTERISTICS					
U_{TM}	Peak on-state voltage	V	1,8	Tvj=25°C, I_{TM}=3,14 I_{TAV}	
$U_{T(TO)}$	Threshold voltage	V	1,1	Tvj=125°C 1,57 I_{TAV}< I_T <4,71 I_{TAV}	
R_T	On-state slope resistance	mΩ	1,8		
I_{DRM} I_{RRM}	Repetitive peak off-state and reverse current	mA	 20 20	Tvj=125°C, U_D = U_{DRM} U_R= U_{RRM}	

CHARACTERISTICS					
Symbols and parameters		Units	T151-100	Conditions	
I_L	Latching current	A	0,5	Tvj=25°C,U_D=12V Gate pulse : 10V, 5Ω, 1 µs rise time, 10µs	
I_H	Holding current	A	0,25	Tvj=25°C,U_D=12V, Gate open	
U_{GT}	Gate trigger direct voltage	V	2,5 5,0	Tvj=25°C, Tvj=-60°C	U_D=12V
I_{GT}	Gate trigger direct current	A	0,2 0,5	Tvj=25°C, Tvj=-60°C	
U_{GD}	Gate non-trigger direct voltage	V	0,25	Tvj=125°C, U_D = 0,67 U_{DRM}	
I_{GD}	Gate non-trigger direct current	mA	10	Direct gate current	
tgd	Delay time	µs	1,6	Tvj=25°C,U_D=500V I_{TM} = 100 A Gate pulse : 10V, 5Ω, 1 µs rise time, 10µs	
tgt	Turn-on time	µs	3,2		
tq	Turn-off time	µs	100÷250	Tvj=125°C, I_{TM}=100 A di_R/dt =10 A/µs, U_R=100V U_D = 0,67 U_{DRM} du_D/dt=50 V/µs	
Qrr	Recovered charge	µC	400	Tvj=125°C, I_{TM}=100 A di_R/dt =10 A/µs, U_R=100V	
trr	Reverse recovery time	µs	16		
I_{RRM}	Peak reverse recovery current	A	50		
$(du_D/dt)_{crit}$	Critical rate of rise of off-state voltage	V/µs	500 1000	Tvj=125°C, U_D = 0,67 U_{DRM} Gate open	
Rthjc	Thermal resistance junction to case	°C/W	0,21	Direct current	

ORDERING							
	T	**151**	**100**	**14**	**7**	**2**	
	1	**2**	**3**	**4**	**5**	**6**	

1. Phase control thyristor.
2. Design version.
3. Mean on-state current, A.
4. Voltage code (14=1400 V).
5. Critical rate of rise of off-state voltage (6 ≥ 500 V/µs, 7 ≥1000 V/µs).
6. Group of turn-off time (du_D/dt=50 V/µs, 4 ≤ 100 µs, 3 ≤ 160 µs, 2 ≤ 250 µs).



Tightening torgue : 12 ÷ 18 Nm
Weight : 150 grams